What Is Claimed Is:

1. A method to facilitate cache coherence with adaptive write updates, comprising:

initializing a cache to operate using a write-invalidate protocol;

monitoring a dynamic behavior of the cache during program execution; and

switching the cache to operate using a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol.

2. The method of claim 1, wherein monitoring the dynamic behavior of the cache involves monitoring the dynamic behavior of the cache on a cache-line by cache-line basis.

3. The method of claim 2, wherein switching to the write-broadcast protocol involves switching to the write-broadcast protocol on a cache-line by cache-line basis.

4. The method of claim 1, wherein monitoring the dynamic behavior of the cache involves maintaining a count for each cache line of the number of cache line invalidations the cache line has been subject to during program execution.

5. The method of claim 4, wherein if the number of cache line invalidations indicates that a given cache line is updated frequently, switching the cache line to operate under the write-broadcast protocol.

6. The method of claim 5, wherein if a given cache line is using the write-broadcast protocol and the number of cache line updates indicates that the given cache line is not being contended for by multiple processors, switching the given cache line back to the write-invalidate protocol.

7. The method of claim 4, wherein if the shared memory multiprocessor includes modules that are not able to switch to the write-broadcast protocol, the method further comprises locking the cache into the write-invalidate protocol.

8. The method of claim 1, wherein the write-invalidate protocol sends an invalidation message to other caches in a shared memory multiprocessor when a given cache line is updated in a local cache.

9. The method of claim 1, wherein the write-broadcast protocol broadcasts an update other caches in a shared memory multiprocessor when the given cache is updated in a local cache.

10. An apparatus to facilitate cache coherence with adaptive write updates, comprising:

an initializing mechanism configured to initialize a cache to a write-invalidate protocol;

an monitoring mechanism configured to monitor a dynamic behavior of the cache; and

a switching mechanism configured to switch the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol.

11. The apparatus of claim 10, wherein monitoring the dynamic behavior of the cache involves monitoring the dynamic behavior of the cache on a cache-line by cache-line basis.

12. The apparatus of claim 11, wherein switching to the write-broadcast protocol involves switching to the write-broadcast protocol on a cache-line by cache-line basis.

13. The apparatus of claim 10, wherein monitoring the dynamic behavior of the cache involves maintaining a count of cache line invalidations initiated by each processor within a shared memory multiprocessor.

14. The apparatus of claim 13, wherein if the count of cache line invalidations indicates that a given cache line is updated frequently in different caches of the shared memory multiprocessor, switching the cache to the write-broadcast protocol.

15. The apparatus of claim 14, wherein if the given cache line is using the write-broadcast protocol and the count of cache line invalidations indicates that the given cache line is being invalidated in only one cache, switching the cache to the write-invalidate protocol.

16. The apparatus of claim 13, further comprising a locking mechanism configured to lock the cache into the write-invalidate protocol if the shared memory multiprocessor includes modules that are not able to switch to the write-broadcast protocol.

17. The apparatus of claim 10, wherein the write-invalidate protocol involves sending an invalidate message to other caches within a shared memory multiprocessor when a given cache is written to.

18. The apparatus of claim 10, wherein the write-broadcast protocol involves broadcasting a data update message to other caches within a shared memory multiprocessor when a given cache is written to.

19. A computing system that facilitates cache coherence with adaptive write updates, comprising:

a plurality of processors, wherein a processor within the plurality of processors includes a cache;

a shared memory;

a bus coupled between the plurality of processors and the shared memory, wherein the bus transports addresses and data between the shared memory and the plurality of processors

an initializing mechanism configured to initialize the cache to a write-invalidate protocol;

a monitoring mechanism configured to monitor a dynamic behavior of the cache; and

a switching mechanism configured to switch the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol.

20. A means to facilitate cache coherence with adaptive write updates, comprising:

a means for initializing a cache to a write-invalidate protocol;

a means for monitoring a dynamic behavior of the cache; and

a means for switching the cache to a write-broadcast protocol if the dynamic behavior indicates that better performance can be achieved using the write-broadcast protocol.